TCAD MODELING OF MIXED-MODE DEGRADATION IN SIGE HBTS

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TCAD MODELING OF MIXED-MODE DEGRADATION IN SIGE HBTS

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

The objective of this work is to develop an effective TCAD based degradation model in predicting the damage that a SiGe HBT undergoes as it is stressed across bias, time and temperature. The material in this work was presented at TECHCON 2013 and IEEE BiCMOS Technology Meeting 2013 and won Best in Session and Best Paper awards respectively [34-35].

In Chapter 1, a brief introduction to SiGe HBTs is presented followed by the motivation for developing a physics based model for the evolution of hot-carrier induced damage in a SiGe HBT. A brief summary of prior work is also presented. In Chapter 2, the effectiveness of the model in predicting the accumulated stress damage in response to time-dependent mixed-mode stress is shown. This is backed by a rigorous calibration of simulation to measurements of impact-ionization and bias-dependent damage. In Chapter 3, a preliminary simulation of mixed-mode damage over temperature is presented. The simulations assume that bulk of the temperature dependence is from the change in impact-ionization rate and that scattering length changes little over temperature. The limitation of this model is presented. In Chapter 4, a detailed temperature-dependent model is presented for capturing the damage behavior of SiGe HBTs along with calibration of simulations to measurements. The temperature dependence of Hydrogen diffusion is incorporated and the resulting physically correct temperature dependence of the scattering-length is shown.

Finally Chapter 5 summarizes the work presented in this thesis and concludes by listing the future research needed in order to get a push-button damage reliability prediction over stress time, temperature and bias.

CHAPTER 1
INTRODUCTION

Silicon Germanium Heterojunction Bipolar Transistor

In the past decade there has been a global increase in wireless communication and as a result several technologies have developed over the years and found a niche to occupy. For high RF performance, high precision analog and even high-speed digital applications, SiGe HBTs have found wide usage because of their ability to deliver III-V like performance using a BiCMOS process that allows good integration. Because of the fact that they are vertical devices, they are less sensitive to the photolithographic node and comparatively offer better performance compared to CMOS at a cheaper cost. Just like CMOS devices, SiGe HBTs too have enjoyed the benefits of scaling including increased speed and performance as shown in Fig. 1.1.

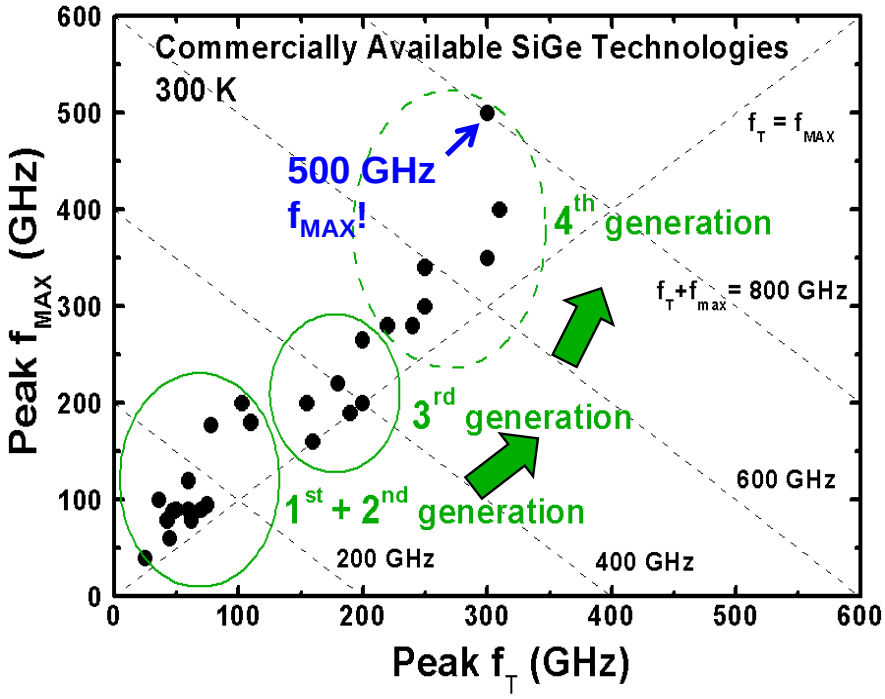

Figure 1.1: The rapid generational evolution of SiGe HBTs with a steady increase in peak f_T and f_{Max}. After [1]

Motivation for Reliability Modeling

With sustained technology scaling, SiGe HBT operating voltages continue to shrink, and device operation is often pushed closer towards the safe operating area (SOA) boundaries, which limit the reliable lifetime of the device. Fig. 1.3 shows the measured SOA boundary for a SiGe HBT. It can be problematic if the critical devices in circuits that require high performance are subjected to mixed-mode (simultaneous application of high current and high voltage) stress and undergo a significant amount of performance degradation within a short period of time.

Classically, the base-current (I_B) reversal point or BV_{CEO} is considered to be a soft voltage limit for the device SOA; however, the same devices are capable of tolerating higher voltages before undergoing noticeable degradation in performance or a catastrophic breakdown. Therefore it is essential to characterize the safe, yet useful, operating regions on the output plane for a device intended to operate beyond BV_{CEO}. This is the region where the device is subjected to a variety of mixed-mode stress mechanisms, leading to device degradation and reduction in the device lifetime.

Moreover, practical applications of these devices in high-performance RF and mixed-signal circuits often demand dynamic operation of the device in various regions on the output plane involving complex damage and annealing mechanisms driven by separate physical processes and their temperature dependencies [2]. Fig. 1.2 shows a typical dynamic load line for a device swinging in a complicated way across the output plane within a power driver circuit. Fig. 1.3 shows the various complicated degrees of damage due to different physical mechanisms as a device operates on different regions across the output plane. Being able to simulate the aging of a circuit is an invaluable tool to any circuit designer and in this approach it is done by first accurately modeling the aging of devices.

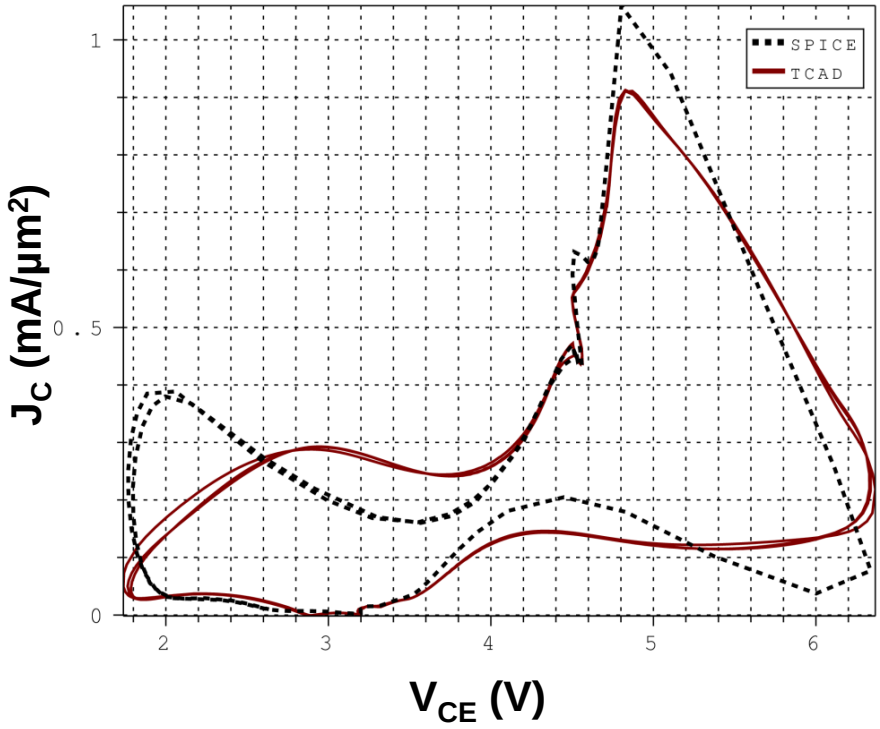

Figure 1.2: Simulated dynamic load line on the output plane for a SiGe HBT operating in a circuit using SPICE and TCAD.

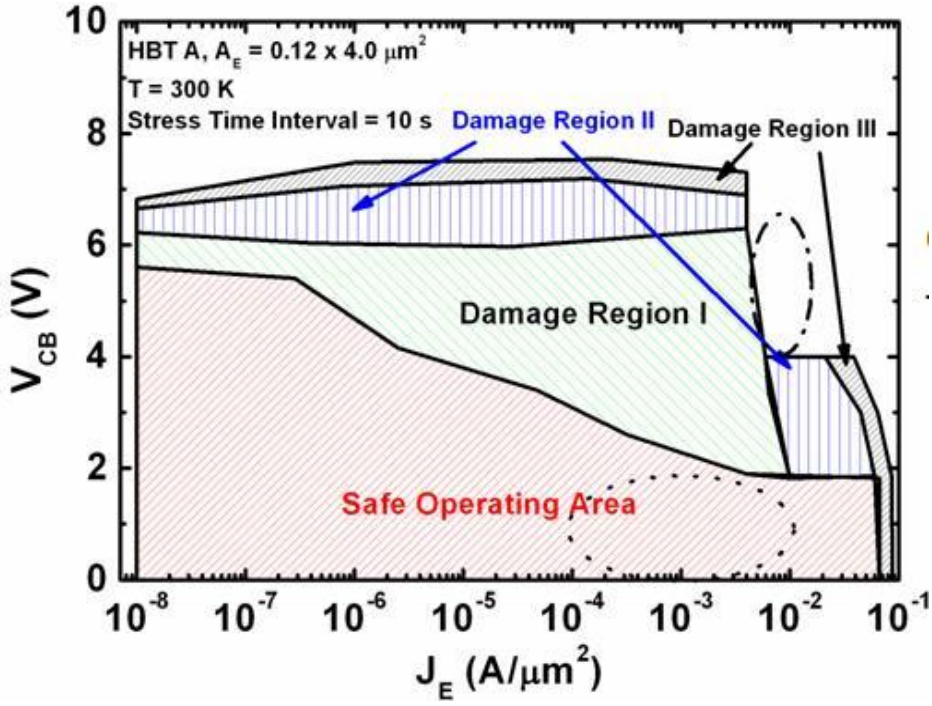

Figure 1.3: Various damage regions bounding the safe operating area of a SiGe HBT on the output plane. The SOA shrinks with technology scaling. After [5]

Prior Work

A physics-based Synopsys Sentaurus TCAD degradation approach was presented in [3] to model the generation and transport of hot carriers from within the device to the different silicon-oxide interfaces, thus enabling robust calculation of time-dependent formation of traps at the various interfaces within the device during stress. The bias-dependence of mixed-mode degradation was modeled and then coupled to extract the transient degradation of a device exposed to a single stress condition as shown in Fig 1.4 [3-7]. Here, the approach in [3] is extended by comparing the simulated and measured damage response accumulated for a single device as it moves over multiple stress points on the output plane, and along different stress paths. Using this approach, an estimation of the accuracy and limitations of the current calibrated TCAD model in predicting the damage response of devices in circuits comprising complex dynamic load lines is achieved. This procedure has significant implications for a robust and reliable performance of SiGe HBTs inside complex circuits.

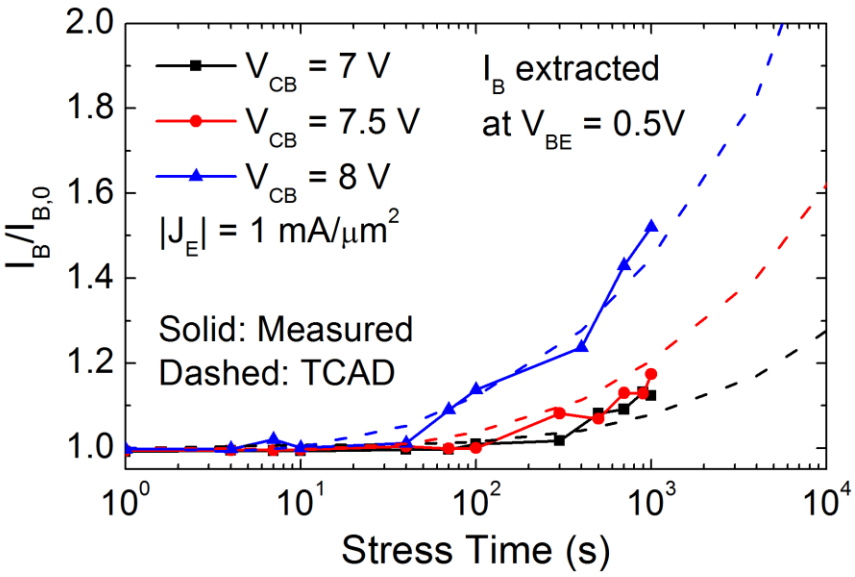

Figure 1.4: Simulated vs. measured change in I_B vs. stress time for a range of V_{CB} stress conditions with J_E = -1 mA/μm^2. After [2]

CHAPTER 2
TCAD SIMULATION OF TIME-DEPENDENT ACCUMULATED STRESS DAMAGE

Damage Physics of Mixed-Mode Stress Degradation

Under mixed-mode stress, minority carriers injected into the collector-base (CB) space-charge region gain energy proportional to the effective electric field and undergo impact-ionization, resulting in creation of energetic electron-hole pairs which further undergo subsequent impact-ionization, leading to an avalanche multiplication process. As shown in Fig. 2.1 these generated secondary and tertiary carriers can in turn propagate to the emitter-base (EB) or shallow-trench (STI) oxide interfaces depending on the momentum of the carrier and the effective electric field (i.e., electron vs. hole). If these carriers have sufficient energy from field acceleration, they can knock off H atoms used to passivate the Si dangling bonds at the oxide/Si interface. This causes H to diffuse away from the interface and cause a net increase in interface traps. This ultimately leads to an increase in base current to compensate for trapping and de-trapping events happening at the interfaces as shown in Fig. 2.2.

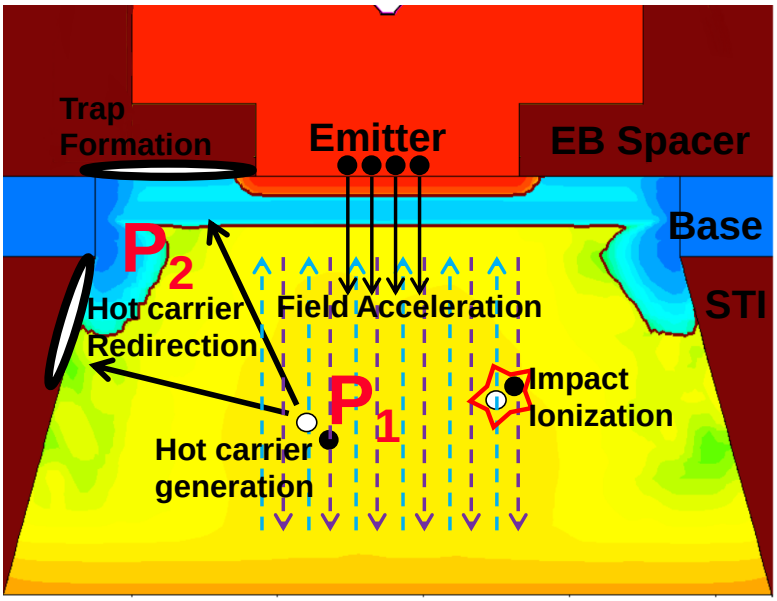

Figure 2.1: Mixed-Mode Damage Process

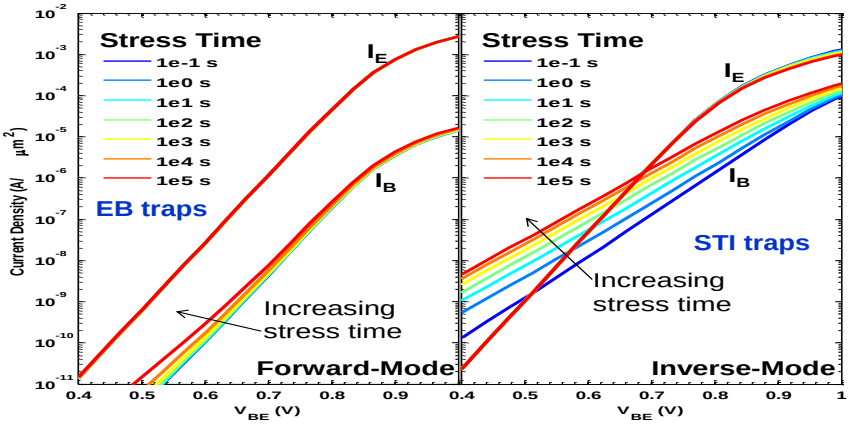

Figure 2.2: Simulated stress response for forward and inverse Gummel characteristics following damage done to EB and STI interfaces with a stress condition of V_{CB} = 8 V and J_E = 1 mA/μm^2.

The "success rates" of these carriers reaching the oxide interfaces are modeled using the lucky-carrier model and depend on a sequence of events [8]. First, a carrier must have sufficient energy to reach the oxide interface and cause the formation of trap (2.1). Second, it must get redirected to the oxide (2.2)[9]. Finally, after having the sufficient energy and being directed toward the oxide, it must not undergo a momentum-robbing collision before reaching the oxide interface (2.3) [10]. Each one of these events is expressed in the model using a probability, and the product of these three probabilities determines the actual trap formation kinetics. Both the actual damage creation mechanism and the associated avalanche generation process of hot-carriers responsible for trap generation at the oxide interfaces are important for this study. The hot carrier energy depends on the effective electric field (F_{eff}) based on hydrodynamic transport. The number of carriers getting generated is determined by the scattering length (λ) for impact-ionization. λ also sets the distance probability. φ_{hot} is the energy required to produce a trap at the interface. λ_r is the scattering length for redirecting collisions.

$$P_{hot,e/h}(\varepsilon, x, y) = \frac{1}{\lambda F_{eff}(x,y)} e^{\varepsilon/\lambda F_{eff}(x,y)} d\varepsilon \tag{2.1}$$

$$P_{red}(\varepsilon) = \frac{1}{2\lambda_r}\left(1 - \sqrt{\frac{\varphi_{hot}}{\varepsilon}}\right) \tag{2.2}$$

$$P_2(x, y) = e^{-d/\lambda} \tag{2.3}$$

Impact-Ionization Calibration

In order to identify the SOA of a device from TCAD it is important to first make sure that avalanche generation (2.4) is calibrated properly, as this is the source for the hot carriers that ultimately cause damage at the oxide interfaces. The Okuto-Crowell impact-ionization model was calibrated to measurements and further used to simulate the avalanche generation process, as it provides a good empirical fit across a wide range of temperatures. Fig. 2.3 shows the calibration of avalanche multiplication across different current injection levels and across temperatures for an NPN device to ensure that the generation of hot carriers participating in the damage physics is accounted well in the output plane. Table 2.1 gives the calibration values. Following this M-1 calibration, the damage model physics can then be calibrated to data for a robust fit in degradation over extended periods of time. Fig. 2.4 shows the simulated damage response obtained from the increase of base leakage in Gummel characteristics measured at V_{BE} = 0.5 V after 100,000 s of mixed-mode stress. Each point represents a fresh device stressed at the associated emitter current density and CB voltage. Two distinct damage regions can be observed from this figure.

$$\alpha(F_{\text{ava}}) = a \cdot \left(1 + c(T - T_0)\right) F_{\text{ava}}^{\gamma} \exp\left[-\left(\frac{b[1 + d(T - T_0)]}{F_{\text{ava}}}\right)^{\delta}\right] \tag{2.4}$$

Table 2.1: Values used in the Okuto-Crowell Model for calibrating Avalanche Multiplication

Symbol	a	b	c	d	γ	δ
Electron	0.43	4.81E+05	3.05E-04	6.86E-04	1	2
Hole	0.24	6.53E+05	5.35E-04	5.67E-04	1	2
Unit	V^{-1}	V/cm	K^{-1}	K^{-1}		

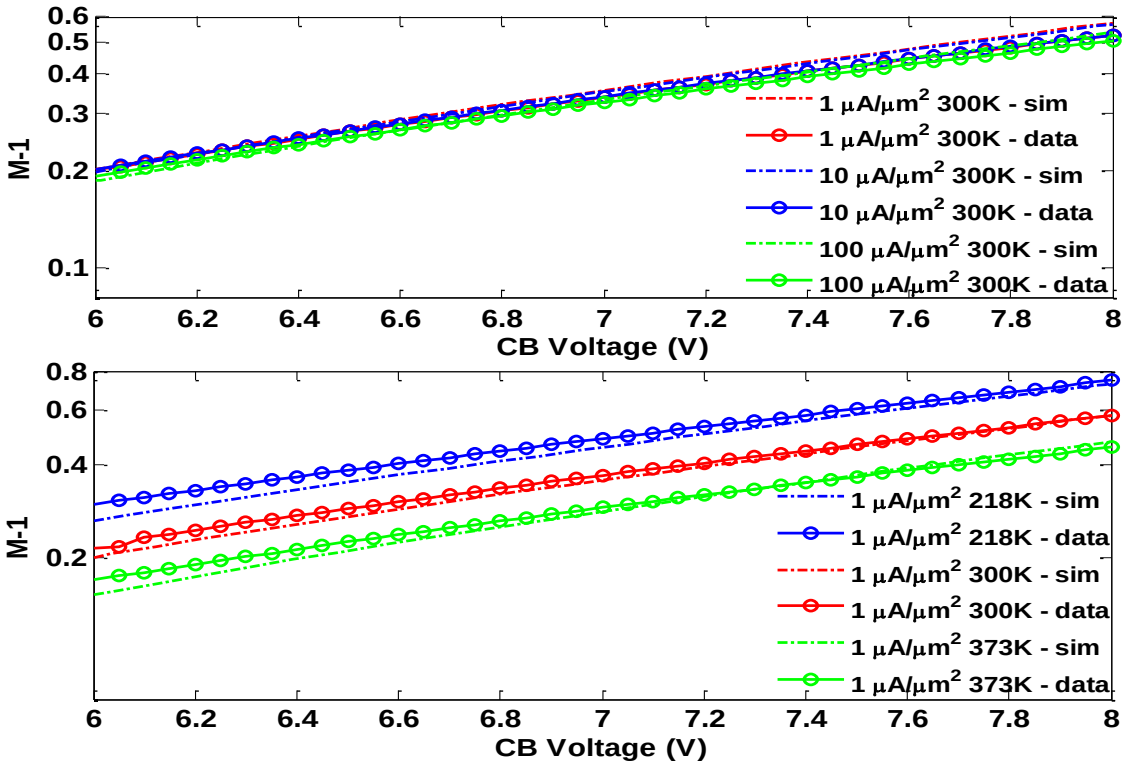

Figure 2.3: Calibration of avalanche multiplication across current levels and across temperatures for an NPN.

The simulated BV_{CEO} is only 3.3 V. However, damage originates from regions of high current and voltage much higher than BV_{CEO} and finally propagates to regions of low current and low voltage over time. Larger stress voltage results in larger avalanche multiplication due to larger electric field at the CB junction and allows for more hot carriers to reach the oxide interfaces. In addition, for low to medium current densities, increasing the emitter current density increases the current injected into the CB depletion region for participation in the avalanche process. However, for high current densities beyond 1 mA/μm^2 the Kirk effect and barrier effect set in. As a result, not only is the peak electric field weaker but it is also pushed deeper into the collector, impeding hot carriers from getting generated and also reaching the EB spacer with sufficient probability to create damage [3]. This is shown in Fig. 2.5.

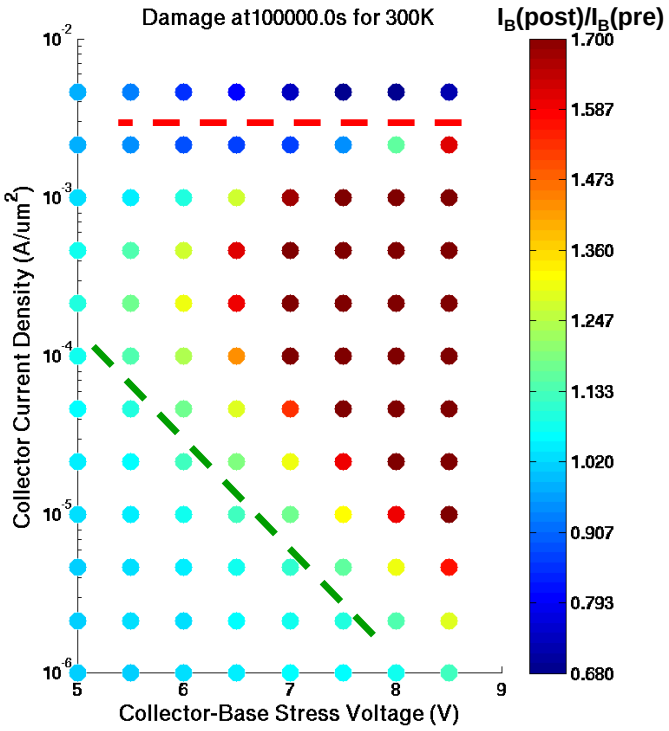

Figure 2.4: Simulated degradation (IB increase) from forward Gummel characteristics at VBE = 0.5 V after 100,000 s of stress at each stress point for an NPN.

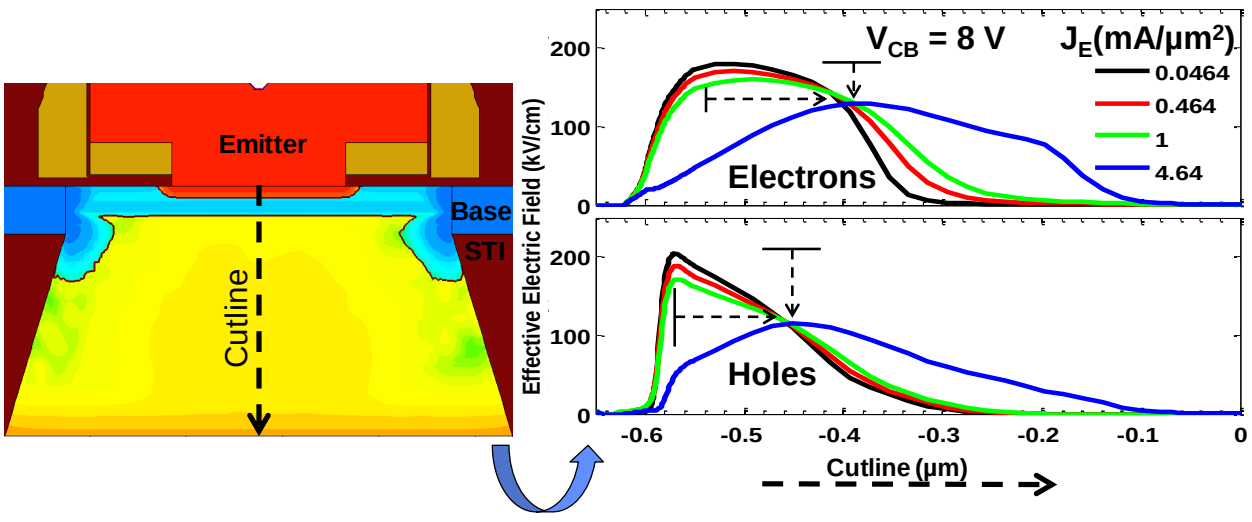

Figure 2.5: Reduction and movement of peak electric field of carriers with the onset of Kirk effect for an NPN. After [3]

The reaction-diffusion (R-D) model is governed by the following equation for both the forward and reverse rate of trap formation within the device [9]:

$$\frac{\partial N_{it}}{\partial t} = K_F(N_0 - N_{it}) - K_R N_{it} H_2 \tag{2.5}$$

As the forward reaction (K_F) gets restricted by high injection effects, the reverse rate of reaction (K_R) starts to dominate and lingers as a negative constant in the equation. This negative constant manifests in the high current density region by annealing existing traps and thereby decreasing the base leakage below unity, as can be seen in Fig. 2.4. However, this region still requires sophisticated models to properly account for the hydrogen diffusion and therefore only the forward-reaction dominated region is presented in this study.

Damage Calibration and Stress Setup

Before making a direct comparison of accumulated damage between measurement and simulation, a boundary needs to be defined where a set of sweep points chosen for stressing has a degradation that is well predicted by the TCAD model. The increase in base current leakage has been used as a measure of damage to calibrate simulations to measurements under forward mode of operation for the NPN SiGe HBT. Fig. 2.6 shows a set of 5 points where calibration was performed to get a good fit between measurement and simulation.

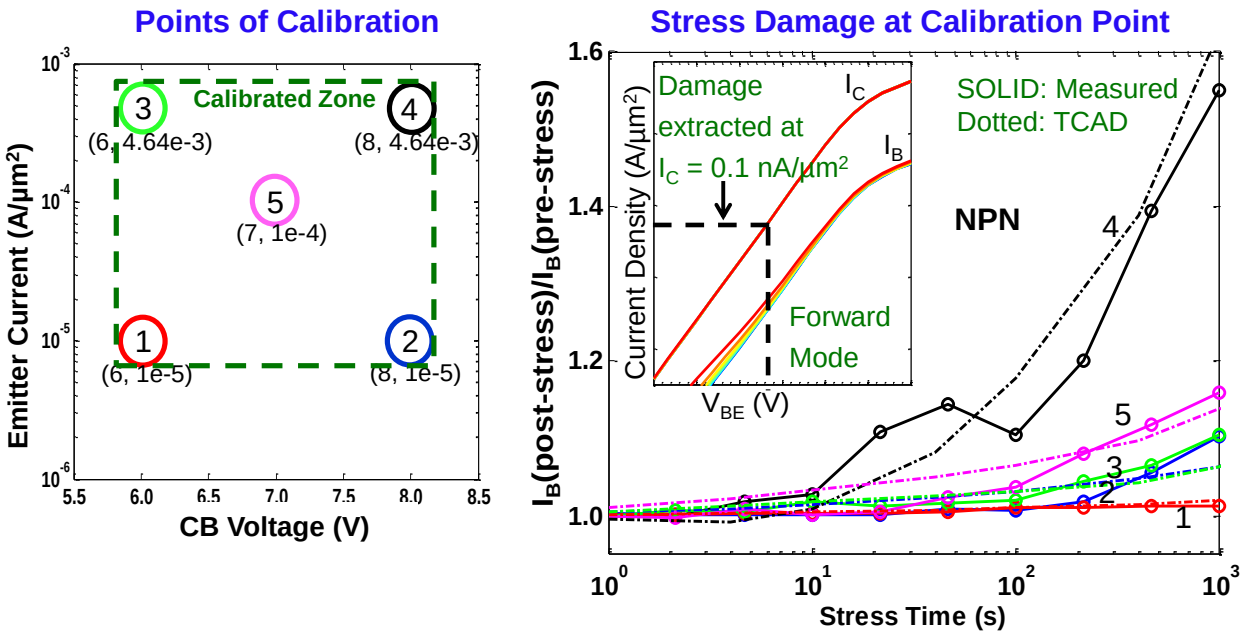

Figure 2.6: 5-points for damage calibration marked with the color codes on the left figure and the corresponding damage curve shown with the appropriate color on the right.

The fit was obtained by calibrating the mean free path of collision for the carriers to 6 nm, similar to what was done in [3]. The calibration points were chosen such that they consist of low to medium current injection and span the voltage range where the impact ionization is also prominent. Within this calibrated zone, 6 points (marked A-F in Fig. 2.7) have been chosen to serve as the set of stress points that a single device will sequentially get exposed to for 1000 s of stress each. Two sweeps were performed using these 6 points: the first starting from point A and ending at point F in a counterclockwise direction, and the second starting from point E and ending at point F in a clockwise direction. Ultimately the future goal of this work is to be able to simulate the damage accumulated over time as a device is swept over any continuous dynamic load line as shown in Fig. 2.7. But before doing that it is crucial to establish that procedure used in this work is valid for even step-wise pseudo-dynamic load lines.

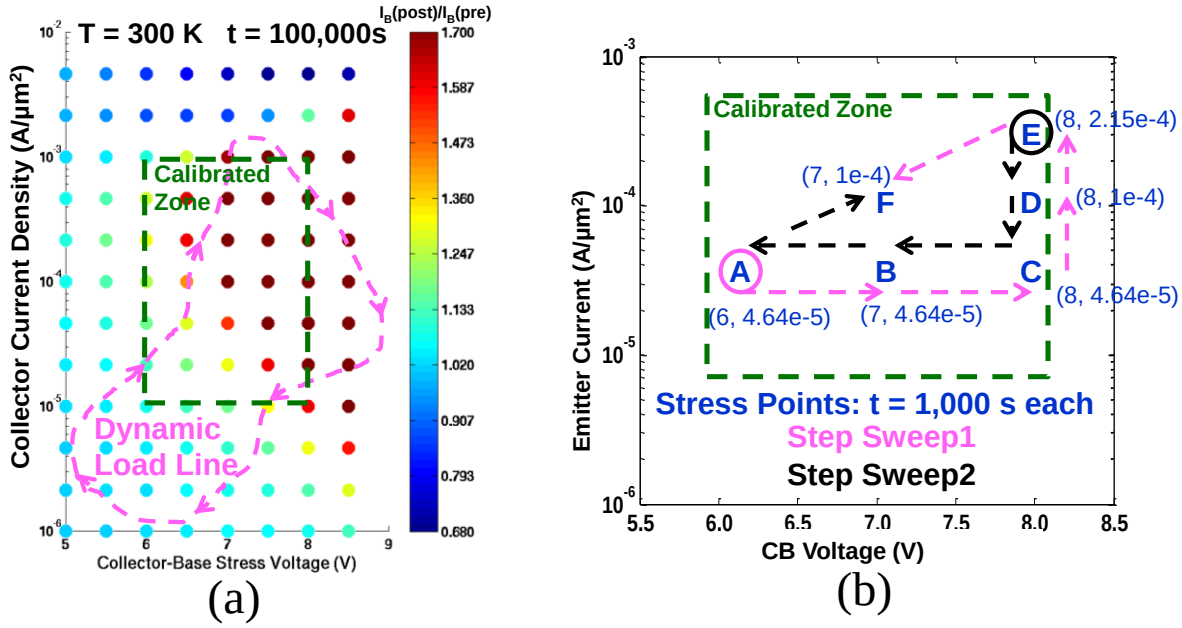

Figure 2.7: (a) Hypothetical dynamic load-line. (b) Stress sweeps used in this study to emulate a pseudo-dynamic load line.

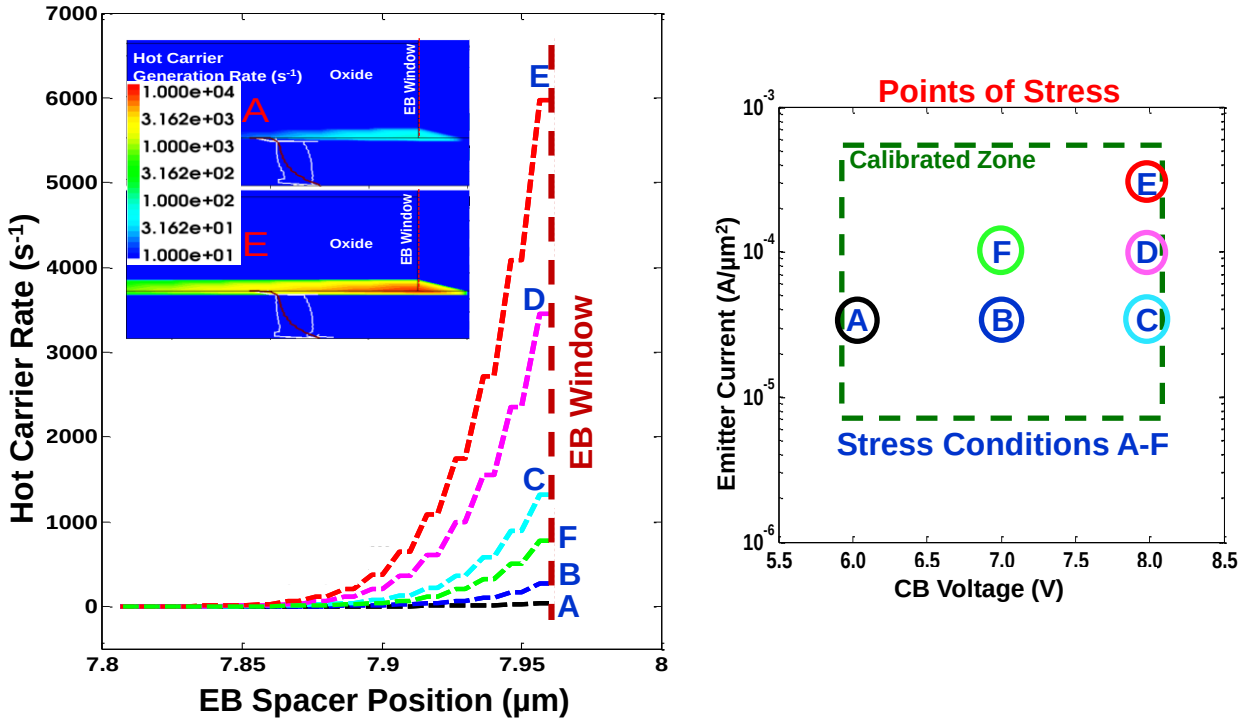

Figure 2.8: Simulated Hot carrier generation rate at EB spacer. 2-D cross-section of the rate for stress points A and E shown as an inset.

Discussion of Accumulated Stress Damage

With the two sweeps starting at the extreme ends of the damage space, point A is expected to accumulate the least amount of damage, whereas point E is expected to accumulate the most amount of damage by having the most aggressive mixed-mode stress condition. This can be seen clearly from the impingement rate of hot carriers at the EB interface in Fig. 2.8. Fig. 2.9 shows the associated accumulated traps over the two different sweeps at the EB interface. As expected, there is a clear bifurcation initially in the accumulated traps generated over time. But most importantly, there is also a clear convergence during the final and common sweep F. Fig. 2.11 shows that the spatial profiles of traps generated for the two different sweeps at the end of 6000 s of stress are virtually identical. Despite being exposed to the same stress points for the same duration, there is no necessity that the two different sweeps must have the same overall degradation. This is because, apart from the dependence on the bias condition, the annealing and trap generation processes are also a function of the existing traps, or in other words, the number of traps that cannot be occupied. However, as the number of available traps to be occupied at the start of the stress sweep is significantly larger than the existing number of traps ($N_0 >> N_{it}$), the following approximations were made to (1) as in [11]:

$$N_{it}(t) \approx 1.16 \sqrt{\frac{K_F N_0}{K_R}} (Dt)^{\alpha} \tag{2.6}$$

This equation becomes invalid when the generated number of traps becomes comparable to the available trap concentration. The fact that there is very little deviation between the numbers of interface traps at the end of the two sweeps, and the continued increase in the trap generation and damage response, suggests that the two sweeps are not limited by the availability of traps in

simulation. In addition, this convergence is promising, in that, even when required to simulate the degradation due to a dynamic load line for a device, a simple integration of traps over time over a continuous set of stress points is indeed plausible and can be path direction independent, as long as the integration is performed in a region where the forward rate of trap formation dominates the reverse rate and the availability of traps is not limiting.

Looking at the damage response from the sweeps in Fig. 2.10 also reveals an initial deviation of paths and a final convergence, in both simulation and measurement, similar to what is present for the interface traps in Fig. 2.9. The errors bars on the measured data represent the bounds of the sample set used and indicate data spread over the wafer. These results experimentally confirm that path independent integration of traps and damage is indeed possible within the zone being studied on the output plane for this device. The results in Fig. 2.9 show that the simulated damage response matches well with the (bounded) data up to about 3000 to 4000 s, validating the calibrations performed in Fig. 2.6, but the data later tapers to a slightly lower damage response value compared to the simulated values. There are two possible reasons to explain this difference. First, the simulations were performed without accounting for the self-heating of the lattice, which can reduce avalanche generation and also the hot carrier generation at the EB oxide. Second, looking at the interface trap concentrations accumulated from the first sweep at 4000 s and for a simulated N_0=5x10^{12} cm^{-2}, the analytical approximation in (2) holds well only up to a N_0/N_{it} ratio of roughly 15 or more. For better correlation for extended periods of time, the existing model can be improved with an iterative approach to reduce the trap generation at a time step based on trap availability ($N_0 - N_{it}$) or by solving the full R-D equation without approximations.

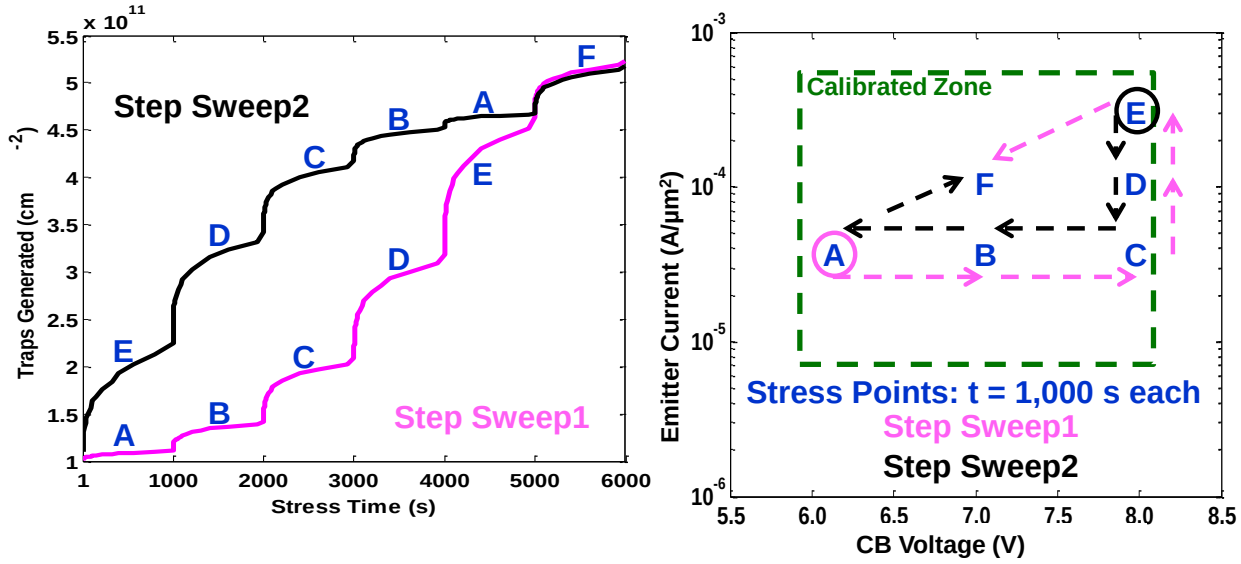

Figure 2.9: Peak Trap concentration at EB spacer over the two different stress sweeps. The stress condition associated with each stress period of 1000 s has been identified with labeling convention from Fig. 2.7.

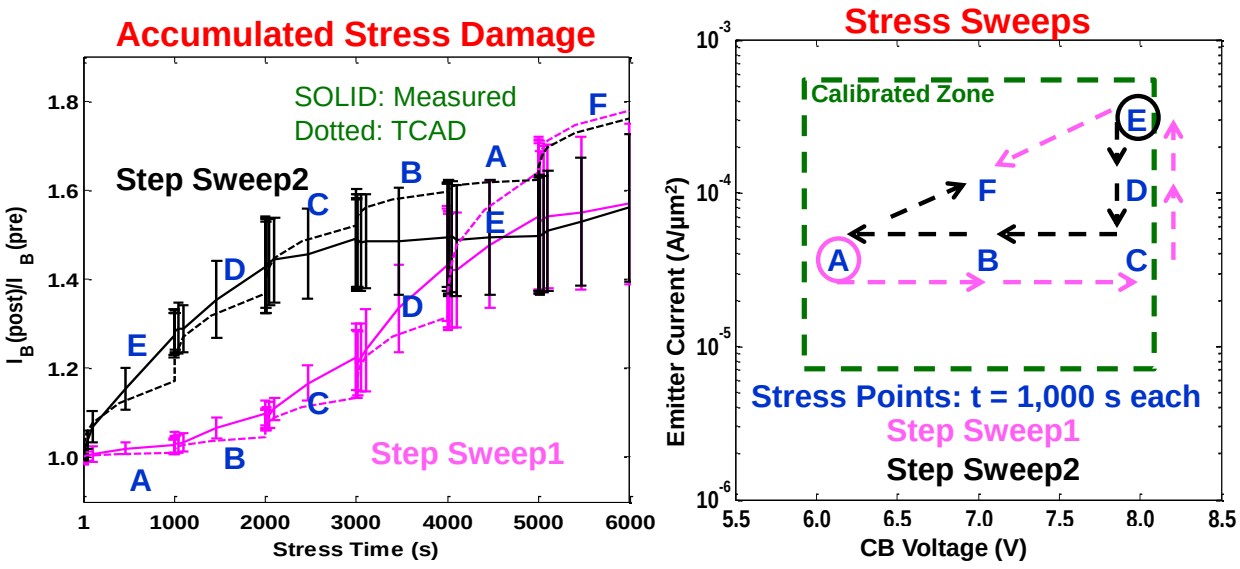

Figure 2.10: Degradation from forward Gummel characteristics at EB spacer over the two different stress sweeps for VBE = 0.5 V. The stress condition associated with each stress period of 1000 s has been identified with labeling convention from Fig. 2.7. The solid lines show the mean value of measured data and the vertical cross-lines show the spread of the data over a sample of six devices for each stress sweep.

Despite the limitations of the current simulation setup, there is sufficient evidence from both measurement and simulation that accumulation of traps correlates well with damage response observable from the base leakage in the forward Gummel characteristics. Therefore, the accumulation of traps is not just limited to discrete point stresses but can next be extended to practical applications in circuits, where the devices are exposed to dynamic load lines consisting of more continuous set of stress points on the output plane.

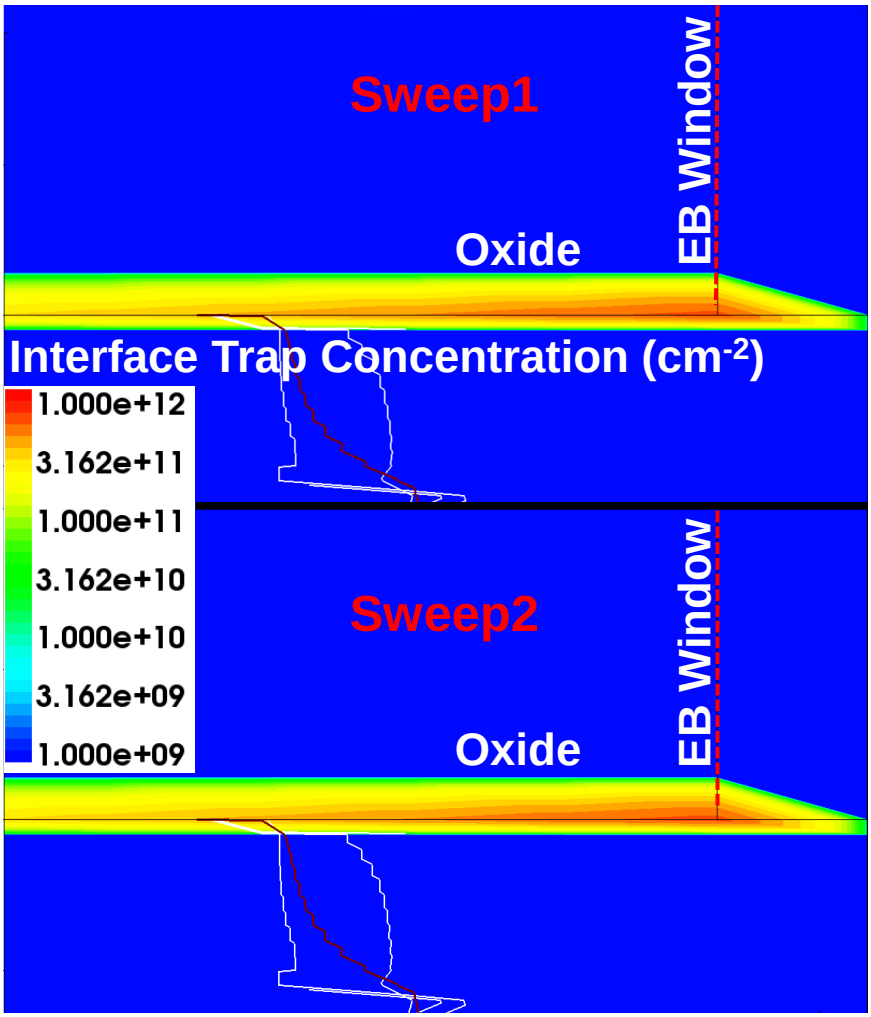

Figure 2.11: Simulated 2D Cross-sections of the total interface trap concentration at the EB spacer after the 6000 s of stress for the two sweeps in Fig. 3. Non-existent spatial difference in trap accumulation after the two stress sweeps.

CHAPTER 3
PRELIMINARY TEMPERATURE SIMULATIONS OF MIXED-MODE DAMAGE

The three probabilities associated with the damage physics are very sensitive to even the slightest changes in the mean-free-path, and can impact the generation of traps at the oxide interfaces. With increasing temperature, the mean-free-path length decreases. Keeping all other parameters constant, a power law (3.1) was initially assumed for the temperature dependence of the mean free path length. Fig. 3.1 shows the different dependencies over temperature and Fig. 3.2 shows the corresponding damage associated with using that particular temperature dependence at 373K. From comparison with data, a temperature dependence of -0.2 achieved the best fit. This shows that the bulk of the temperature dependence for stress damage comes from avalanche generation and the temperature variation of mean-free-path length is only minimal.

$$\lambda = \lambda_{300K}\left(\frac{T}{300K}\right)^{exp} \tag{3.1}$$

Despite the large disparity in degradation between the damage contour maps at two different temperatures, the actual hot carrier generation rate decreases only minimally, as can be seen in Fig. 3.3. However, integrating the disparity in hot carrier generation rates at the two different temperatures over time manifests as a large disparity in accumulated traps over time, as shown in Fig. 3.4. The number of traps created in the device is a real measure of damage in the device and is proportional to the base leakage current. Thus, the difference in the accumulated traps shows up as a noticeable difference in the device leakage and shifts the SOA boundary to a higher voltage for a high temperature stress as seen in the difference between Fig. 3.5 and Fig. 3.6.

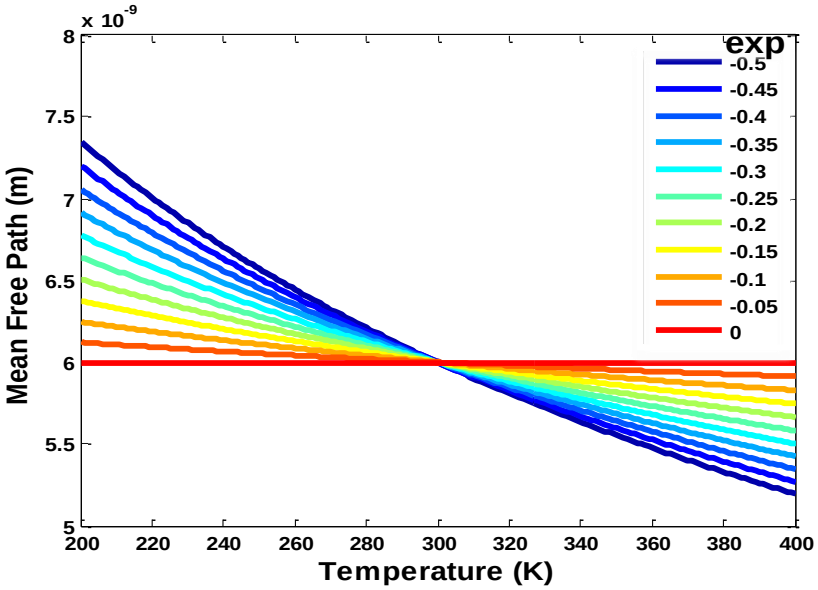

Figure 3.1: Variation of λ over temperature for different power law exponents.

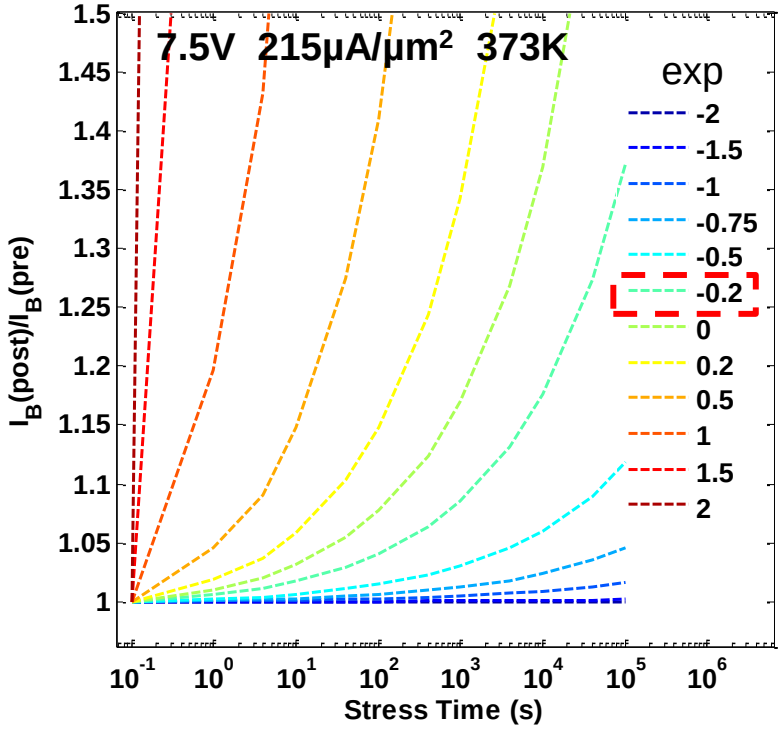

Figure 3.2: Simulated base current degradation over time for different power law exponents at 373 K.

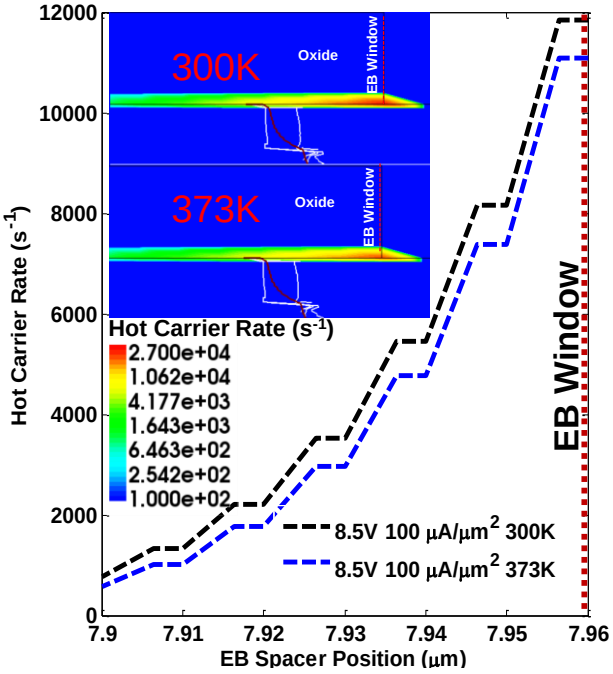

Figure 3.3: Hot carrier impingement rate at the EB spacer oxide for the same stress condition at two different temperatures.

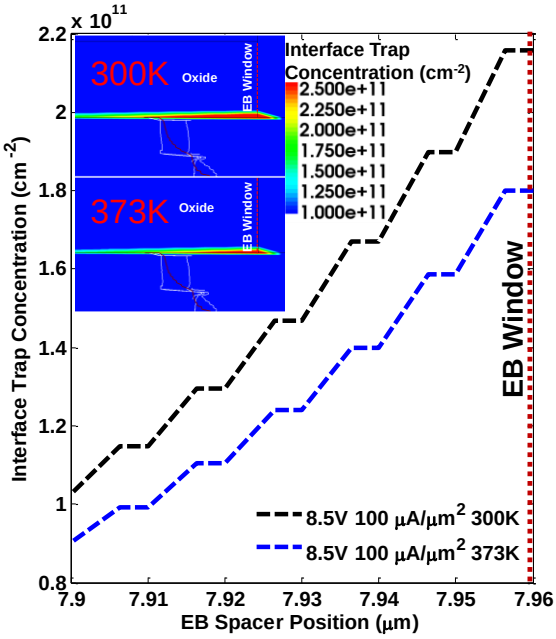

Figure 3.4: Interface traps formed after 1000s of stress at the EB spacer oxide for the same stress condition at two different temperatures.

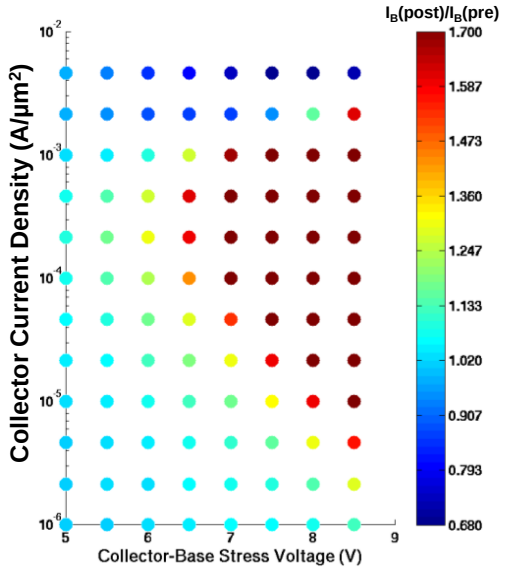

Figure 3.5: Damage contour map from forward Gummel characteristics for 300K extracted at I_C = 0.1 nA/μm^2 after stressing for 100,000 s.

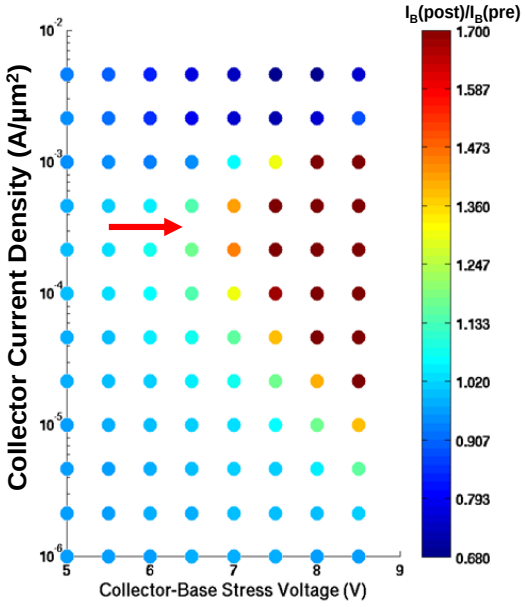

Figure 3.6: Damage contour map from forward Gummel characteristics for 373K extracted at I_C = 0.1 nA/μm^2 after stressing for 100,000 s. SOA shifted to a higher voltage due to reduced hot carrier generation.

Discussion of Results

There are several limitations with this preliminary model for simulating temperature dependence of mixed-mode damage. The simulations performed above assumed that all parameters other than the mean-free path length are constant over temperature. That is definitely not the case. Diffusion of Hydrogen species away from the silicon-oxide interface is exponentially dependent on temperature. Taking that into consideration would allow a greater flexibility in fine tuning the simulation to measurements and would reduce the sensitivity of interface damage to mean-free-path length. Changes to mean-free path length would result in exponential changes in the hot carrier impingement rates at the interfaces at each temperature. But this exponential change can be nullified by the exponential change of the hydrogen diffusion constant and allow for a moderate tunable change in damage. This will be addressed in Chapter 3.

CHAPTER 4

MODELING TEMPERATURE DEPENDENCE OF MIXED-MODE DAMAGE

The net temperature dependence of damage response to mixed-mode stress is a product of three steps. First, impact-ionization being the generation source of hot carriers is a temperature dependent process. Next the fraction of hot carriers reaching the oxide interfaces is also a temperature dependent process governed by the mean-free-path length between collisions for hot carriers at each temperature. Lastly the diffusion of hydrogen away from an interface is also a complex temperature dependent process. The temperature dependence of impact-ionization was already shown in the calibration of measurements to data in Fig. 2.3 and Table 2.1. In this section the models used for hydrogen diffusion and the temperature dependence of mean-free-path length will be discussed.

Hydrogen Diffusion in Silicon

Hydrogen in a crystalline lattice produces two kinds of traps. One is a shallow level trap associated with a Hydrogen atom occupying an interstitial site (also called Bond Center or BC) of a bond between two Silicon atoms. The other trap is a deep level trap associated with a physical bond between a Silicon atom and a hydrogen atom. Just like the dichotomy in states due to the formation of conduction and valence bands in a semiconductor, hydrogen in crystalline Silicon system manifests itself as a system of two states [12-13]. Each state has an energy distribution centered on the peak trap energy as shown in Fig. 4.1. At the minimum between the two energy distributions of trap states lies the chemical potential of Hydrogen. Below this energy

level, hydrogen trap states are mostly occupied and above this level, the traps associated with the dangling bond are mostly empty.

In order for interstitial diffusion of hydrogen to take place, the hydrogen atom must gain sufficient energy to get promoted to the saddle point for migration. Hydrogen diffuses by hopping over an energy barrier E_M from one interstitial site to another. This energy E_M takes on values from 0.2eV to 0.6eV depending on the process that was used to grow the Silicon and embed the hydrogen [13]. In this study the following Arrhenius relationship is used with $D_0 = 9.41 \times 10^{-3}$ cm^2/s and $E_M = 0.48$ eV to take into account the thermally activated process of interstitial diffusion after [14]. The following behavior introduces temperature dependence into the interface trap creation equation (2.6):

$$D(T) = D_0 e^{-E_M/k_B T} \tag{4.1}$$

Hydrogen diffusion at an oxide-Silicon interface is a two-step process. First a hydrogen atom must get liberated from a Si-H bond to create a dangling bond and occupy an interstitial site. Then only the hydrogen atom can start diffusing. The energy of the trap associated with a dangling bond (E_{Si-H}) is 1.9-2.5eV below the energy for the Bond Center (E_{BC}) depending on the temperature at which the interface was passivated [15-17]. A higher passivation temperature results in a dangling bond trap with a lower energy with respect to the free space energy of Hydrogen. Therefore a higher passivation temperature increases the spacing between E_{BC} and E_{Si-H}. In this work the activation energy required to promote a deep trap to a shallow trap was assumed to be 2.3 eV following the analysis in [9]. Although a transition of a hydrogen atom from a deep trap to a shallow trap is happening in energy, the actual transition must happen physically by breaking a Si-H bond, leaving a dangling bond behind and subsequently moving

the hydrogen atom to the nearest Si-Si interstitial site. The physical movement is a diffusion limited step and is temperature dependent. At very low temperatures the hydrogen atom has great difficulty in making the spatial transition and therefore has great difficulty in making the transition from E_{Si-H} to E_{BC} even when supplied with sufficient energy. The only way to increase the chances of creating a trap at low temperatures is by bombarding the interface with more hot carriers. Despite the reduction in diffusion constant, more traps are created at low temperatures in a SiGe HBT because of the increase of hot carriers reaching oxide interfaces due to the increase in mean-free-path length below 300 K.

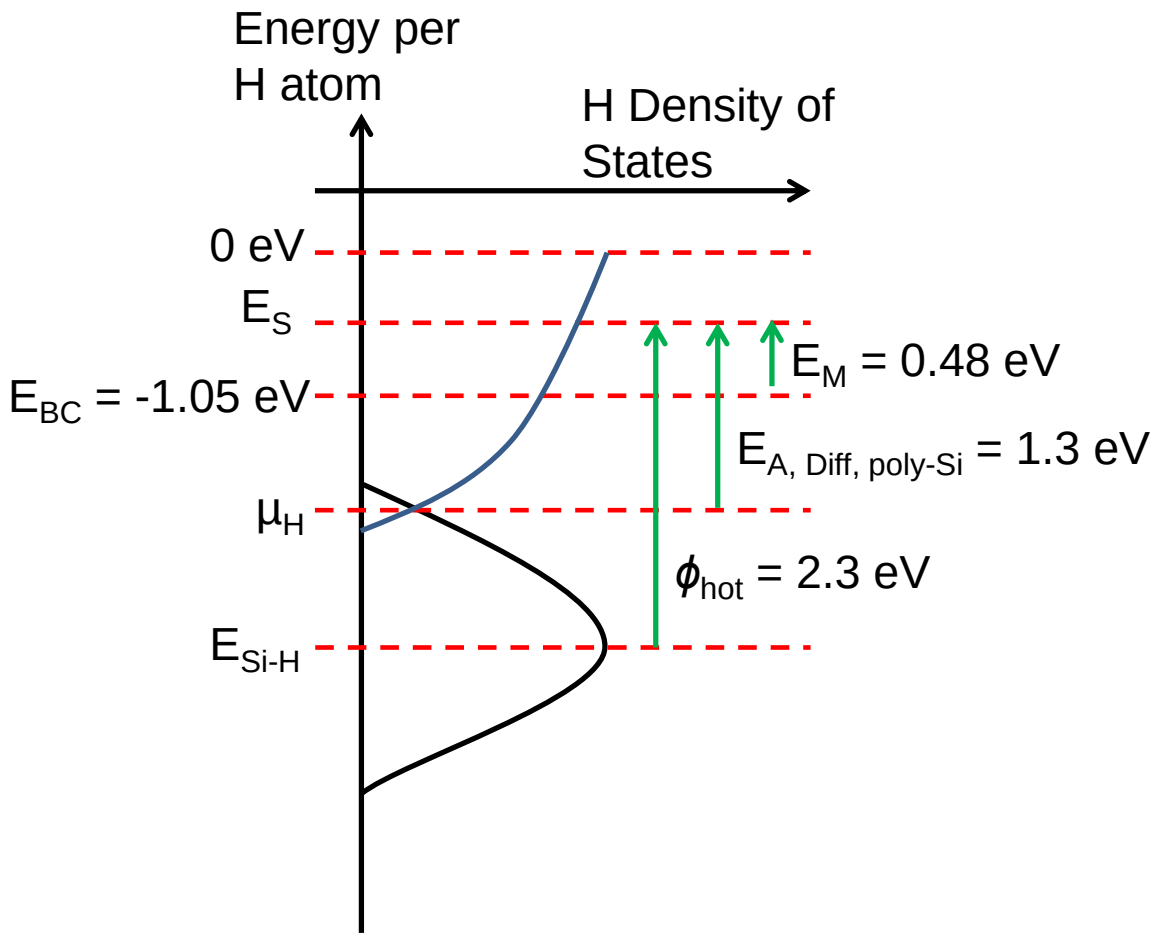

Figure 4.1: Distinct trap states in Silicon and the associated activation energies required for diffusion of hydrogen.

Temperature Dependence of Mean-Free-Path

In the damage physics model for the SiGe HBT, the three probability equations (x – y) involve two different mean-free-path lengths (λ and λ_R). λ is an average of optical phonon scattering, impact-ionization and long-wavelength acoustic phonon scattering. λ_R is an average of long-wavelength acoustic phonon and intervalley scattering [18]. Optical phonon scattering is the dominant inelastic scattering suffered by carriers in the collector-base space charge region resulting in impact ionization. On the other hand in order for a carrier to get redirected, an elastic collision must take place between the lattice and carrier. Redirecting collisions happen with a lesser frequency and therefore λ_R is a factor of 5 - 10 larger than λ at room temperature [19]. However the exact value of λ_R is not as significant since λ is a more sensitive parameter being involved in exponentials.

To minimize any scattering of carriers from a crystalline Silicon lattice the ideal temperature to operate is 0 K. At very low temperatures the maximum mean free path length (λ_0) is determined based on the geometry of the lattice. As the temperature is increased, phonons are introduced into the lattice with different harmonics and start to interact with one another and also with the flow of carriers. The operating temperature is directly proportional to the number of phonons introduced. The number of phonons in the lattice is directly proportional to the collision frequency of phonons in the lattice. As collision frequency increases with temperature, the mean distance traveled by a carrier decreases inversely. Thus at very high temperatures the mean free path length is expected to drop as T^{-1}. The exact temperature dependence for both mean scattering lengths are given as follows [18-19]:

$$\lambda(T) = \lambda_0 \tanh\left(\frac{E_p}{2kT}\right) \tag{4.2}$$

This inverse temperature dependence of mean-free-path length was observed when calibrating the measured damage to the simulated damage using different mean-free-path lengths for different temperatures. Fig. 4.2 shows the calibration of mixed-mode damage across three different conditions. A stress condition in the impact-ionization dominated region was chosen such that enough damage could be observed within 1000s across the three temperatures. Fig. 4.3 shows a good correlation between a T^{-1} curve and the mean-free-path lengths used at three temperatures for calibrating mixed-mode-damage. Fig. 4.4 shows the hot carrier rates at each temperature. The exponential reduction in hot carrier rates with temperature was enabled by the exponential enhancement of the diffusion coefficient. Although there is increased damage at 218 K, this behavior is not expected at lower temperatures because of the saturation of λ due to geometrical limits.

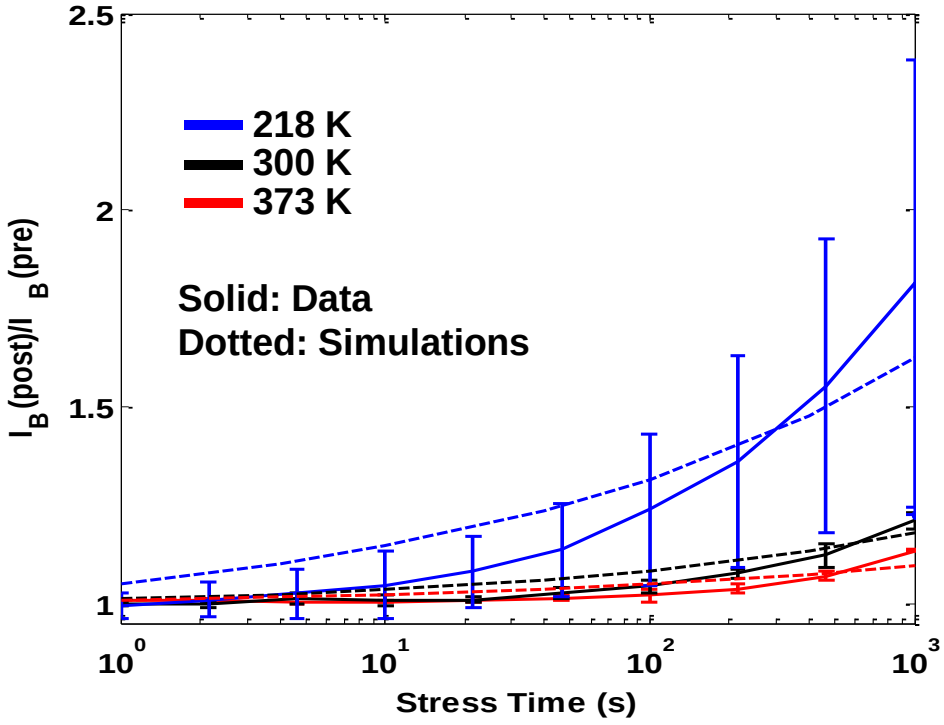

Figure 4.2: Calibration of simulations to measurements for I_B degradation over temperature for a stress condition of stress condition of V_{CB} = 8.5 V and J_E = 0.464 mA/μm^2. Vertical error bars show the spread of data.

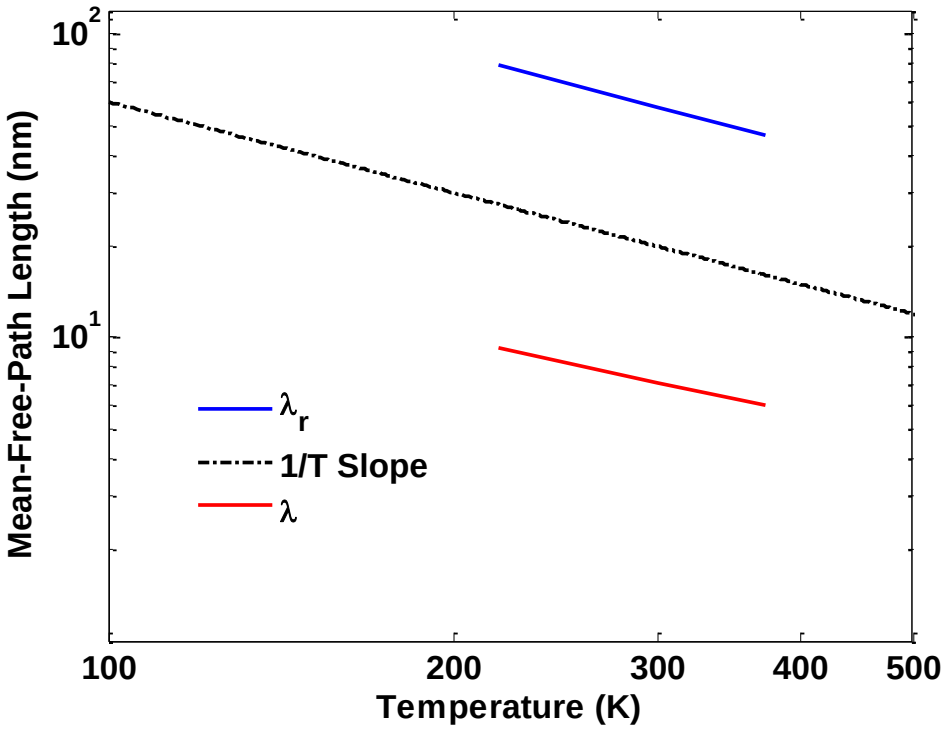

Figure 4.3: Temperature dependence of λ and λ_R. Values used for simulations in Fig. 4.2.

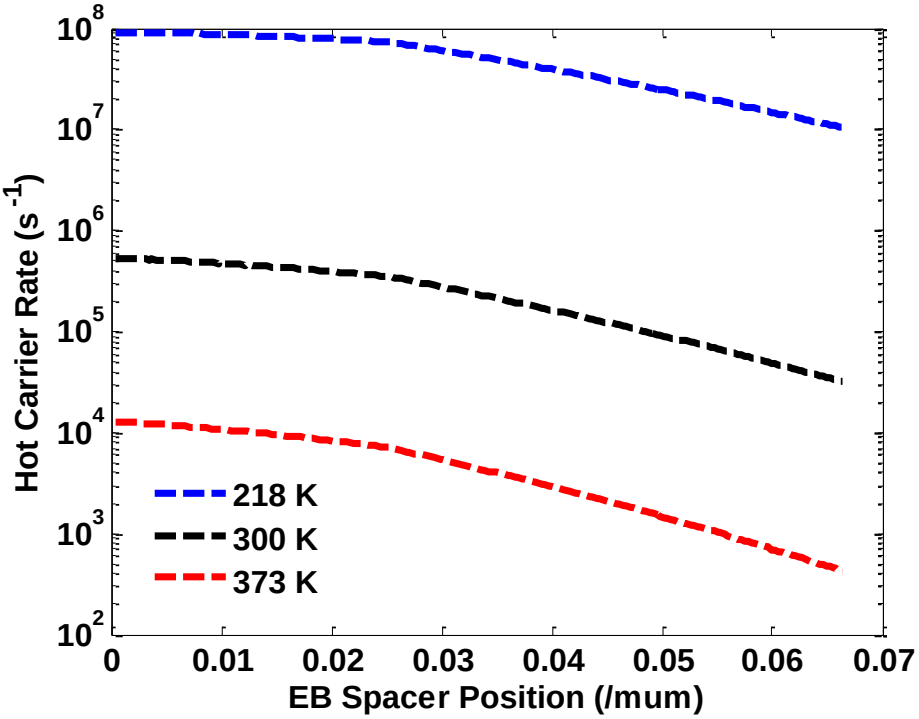

Figure 4.4: Simulated Hot carrier impingement rates over temperature.

Discussion of Results

Although equation (2.6) was originally derived in [9] for a CMOS gate oxide interface, it indeed works well across bias and temperature for a SiGe HBT's EB oxide spacer interface and can be improved as follows. It is first important to note that the Si interface underneath a MOS oxide is crystalline and was likely passivated by diffusing hydrogen through the oxide. As a result, there is not much hydrogen within bulk Silicon. In a SiGe HBT, the silicon of the extrinsic base underneath the EB spacer is usually grown epitaxially and can either be crystalline or polycrystalline and have a lot of hydrogen content as a result of the growth process. Thus the concentration gradient points from the silicon to the oxide. Hydrogen in the oxide has an enhanced diffusion constant compared to the one in silicon as shown in Table 4.1. Because of this, the limiting diffusion constant for replenishing hydrogen at the interface is that of Silicon and is responsible for the initial trap generation at the interface.

In both Fig. 2.6 and Fig. 4.2 despite using $\alpha = 0.25$ factor for time dependence of trap generation derived by Jeppson and Svenssson, it is very evident that the simulation starts to show damage well before the measurements start showing any damage. A possible reason for this discrepancy is that traps that are initially created at the interface are very quickly annealed by hydrogen diffusing from the extrinsic base. This is possible depending on the initial hydrogen concentration at the oxide-silicon interface. For a polycrystalline extrinsic base, the E_A for diffusion is much smaller compared to that for crystalline silicon. Hydrogen atoms located along grain boundaries in the polysilicon or in interstitial Si-Si sites within the bulk material diffuse with an activation energy referred from the hydrogen chemical potential μ_H to the migration saddle point energy E_S. This activation energy is still considerably less than the activation energy ϕ_{Hot} required to dislodge a lone hydrogen atom at the interface of a MOSFET to create a Si

dangling bond because when there is diffusion happening, hydrogen atoms are constantly being replaced. But when there is only one hydrogen atom, that is not the case and the full activation energy from the deep trap level must be supplied. Since this diffusion is a temperature controlled process we see that at lower temperatures, hydrogen within the extrinsic base has great difficulty in reaching the oxide-Silicon interface and is unable to simultaneously anneal traps that are formed. Therefore damage starts to increase much sooner at lower temperatures in measurements.

If the bulk diffusion of hydrogen from Silicon to the oxide interface is not taken into account, the simulation will grossly overestimate the traps being formed at the initial time steps. In addition the calibration performed will be assuming a slower hot-carrier impingement at the interface of hydrogen into the oxide. Both of these are incorrect and will need to be fixed when an annealing model (out of the scope of this work) is implemented. Using a higher α in (2.6) factor might give good match between data and simulation for short stress time periods. But over long periods this will overestimate the trap formation. In [20] $\alpha = 0.3$ was used to fit the base leakage degradation to empirical aging models. However it is important to note that the time dependence of $\alpha = 0.25$ was derived for interface trap formation and should not be confused with base leakage degradation at a given V_{BE}.

Table 4.1: Diffusion of different species Hydrogen in different mediums at T = 105°C indicating diffusion in SiO2 > Diffusion in Poly-Si > Diffusion in Si >> Diffusion in SiN. After [30]

Diffusing Species	H_2	H_2	H	H	H_2	H_2	H^+, H^0	H_2	H, H_2	H, H_2
Diffusion Medium	SiO_2	SiO_2	SiO_2	SiO_2	Poly -Si	Poly -Si	c-Si	c-Si	SiN	SiN
Distance diffused (nm) in t=1s	4.8e2	2.3e1	8.4e4	1.5e4	5.9 e-1	9.4 e1	3.5 e-1	3.7 e1	9.9e-4	7.8e-14
Reference	[21]	[22]	[23]	[24]	[25]	[26]	[27]	[26]	[28]	[29]

CHAPTER 5
CONCLUSION AND FUTURE WORK

After a rigorous calibration of the impact-ionization across bias in the CB junction and a multi-point calibration of the damage response on the output plane, it has been demonstrated that it is possible to model the accumulated stress damage over not just a single bias point but over multiple stress points using the physics-based degradation approach within TCAD. Restricting the region of the study in the output plane to a region that is dominated by the forward trap formation reaction, and comparing the measurements with simulations provide some key insights: 1) the trap generation and the damage response can be integrated over time, independent of the sequence of stress points, and 2) the accumulated stress will still end up with the same number of traps and similar degradation as long as trap availability is not an issue. Noticing the importance of high electric fields for trap formation, SOA boundaries at the low-voltage/low-current values and high-current were identified, with the latter boundary showing the most resilience to time and temperature. The calibrated TCAD model used in this study has been demonstrated to have a very good correlation with measurement in regions of the output plane that are dominated by high-electric field damage. This gives promising information about reliability in practical circuits that operate with SiGe HBTs under time-dependent mixed-mode stress conditions. The TCAD reliability of devices in such circuits can be modeled predictably using this degradation model.

The calibration of impact-ionization model over temperature initially enabled understanding the dynamics of the temperature dependence of the SOA of a SiGe HBT. The temperature dependence of the SOA was investigated by examining avalanche multiplication and the hot carrier generation rate at oxide interface. The preliminary simulations indicated a sharp dependence of damage formation on the mean-free-path length and thus a slow variation of

mean-free-path length over temperature. Similarly, a strong dependence on the hot carrier rates for interface trap concentration over time at the oxide interface was also observed. The model was then further improved to include the physically correct Arrhenius T dependence for hydrogen diffusion and T^{-1} dependence of mean-free-path length to get a tunable calibration with measurements. This is encouraging as the model can not only determine safe operating bias levels for devices but can further be used to perform reliability simulations of SiGe HBTs used in practical application circuits requiring a dynamic biasing and over-temperature operation.

With the forward reaction of the reaction-diffusion mechanism understood, modeled and charted accurately, solving the R-D equation without approximations by properly modeling the reverse reaction will next allow accurate prediction of higher current stress, where the effect of temperature, self-heating and diffusion of the released hydrogen atoms from traps will play a large role on the annealing of traps in addition to the existing degradation model. The reverse reaction or the annealing of traps is assumed to be constant in this study and requires better models to understand the damage physics during high-injection. Although damage recovery (annealing) of traps is seen from the damage contour maps, this region requires solving for the full reaction-diffusion equation (2.5).

The simplification (2.6) was used in this study assuming the forward rate of trap formation is much larger than the reverse rate of reaction [11]. However, it is not applicable in the high-current limit. Additionally, the present study has only considered DC stress to construct the SOA maps. However, the practical application of devices requires dynamic operation across a wide range of voltages and currents. Although a point stress response cannot be directly compared to a dynamic stress response, DC stress degradation still serves as a quick check for device reliability in circuit-level operation. If the actual traps are indeed directly correlated to the

measured leakage in a device, then the damage accrued over a dynamic load-line can simply be calculated by integrating the damage formation rate at each point on the output plane over time.

The damage formation rate is determined mostly determined by the stress bias and temperature. In this study only the mixed-mode stress was used to damage devices. However there are two other stress conditions for SiGe HBTs which also produce hot carrier damage. Reverse EB stress damages devices more aggressively due to the presence of much larger electric fields at the EB junction compared to the CB junction. High current low voltage stress produces damage by means of Auger recombination as opposed to high electric field driven damage [31-32]. Having a unified model that can reliably calculate the damage for a device operating over any of the three stress conditions is vital to achieving push-button reliability prediction for SiGe HBTs and circuits. The current model will need to be adapted to reliably predict the damage behavior for the other stress conditions.

The current work primarily investigated only NPN devices. However PNP devices are also equally important in high-speed analog designs involving push-pull configurations. Any differences between holes and electrons leading to differences in the values used for parameters in the damage physics model need to be investigated. Also the current work assumed a mid-gap level trap state to calculate the recombination current as an approximation. However practical interfaces have multiple energy distributions of traps with donor and acceptor varieties depending on the quasi Fermi level [33]. The issues mentioned above will be addressed in future works.

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